Notice of Allowability	Application No.	Applicant(s)	
	10/074,455	EL-GHOROURY, HUSSEIN S.	
	Examiner	Art Unit	
	Albert W. Paladini	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *applicaatin filed on* .

2. ☒ The allowed claim(s) is/are *1-23*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 4/02,7/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Reasons for Allowance

1. The following is an examiner's statement of reasons for allowance: None of the references cited or the art searched disclose or teach alone or in combination the method or system for designing and implementing a matched instruction set processor by decomposing the instruction set processor into interconnected design vectors which include a binding header method, a run method, a conjugate virtual machine, a binding trailer method and an invocation method.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Relevant Prior Art

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Baror (4926323) discloses an instruction processor whose architecture is based on a combination of a unique system interface, register file and branch target cache. The system interface provides separate address, instruction and data buses. The instruction bus is adapted to receive instructions from an external storage device. The data bus is adapted for bi-directional transfer of data between the processor and external storage device. The address bus is shared between the instruction and data accesses and is implemented in a pipeline fashion so that it can be released before an instruction or data transfer is completed. This allows a subsequent access to begin before the first is completed and allows the processor to have two accesses in progress simultaneously. The register file is included with the processor and contains a plurality of general-purpose registers allowing most instruction operands to be fetched without the delay of external access. The register file incorporates several features, which aid the retention of data required by an executing program, including stack pointer addressing and register bank protection.

Tremblay (6021469) discloses a hardware virtual machine instruction processor, which directly executes virtual machine instructions that are processor architecture independent. The hardware processor has high performance; is low cost; and exhibits low power consumption. The hardware processor was designed primarily for portable applications.

Evoy (6085307) discloses a multiple processor circuit arrangement, which includes a slave processor and a master processor. The slave processor includes a control unit configured to process instructions received by the slave processor, an internal control register arrangement configured to provide at least one of several operational states for the slave processor, a program counter register in the internal control register arrangement configured to point to an address of a next instruction to be processed by the control unit, and a control register access port coupled to the internal control register arrangement to provide external access thereto. The master processor is coupled to the slave processor, and is configured to selectively start execution of the slave processor with a predetermined operational state by writing data into the internal control register arrangement through the control register access port to modify the program counter register.

Elmer (6324638) discloses a vector processor having tens or hundreds of identical Arithmetic Logic Units (ALUs) for processing multiple variable-length vectors in parallel. That is, each ALU processes a different one-dimensional vector in a pipelined fashion, and all ALUs operate concurrently. This architecture, while specifically tailored to scientific computing and thus avoiding some of the complexity of prior architecture, is not optimal for performing a broad range of non-numerically intensive applications. In accordance with the present invention, the computational capabilities of the PowerPC.TM. architecture have been expanded by the inclusion of an additional vector execution unit that operates concurrently with the other execution units on a single instruction stream. In contrast to the vector processing architecture described above, the vector execution unit within the architecture can concurrently process all elements of one-dimensional fixed-length vector operands in parallel rather than one element at a time. The addition of vector processing capability to the general-purpose architecture further accelerates its performance when executing numerically intensive software applications.

Ganapathy (6446195) discloses a multiple application specific signal processor, which includes a instruction, set architecture where dyadic DSP instructions, are provided within gateways in communication systems to provide improved voice and data communication over a packetized network. Each ASSP includes a serial interface, a buffer memory, and four core processors for each to simultaneously process multiple channels of voice or data. Each core processor preferably includes a reduced instruction set computer (RISC) processor and four signal-processing units (SPs). Each SP includes multiple arithmetic blocks to simultaneously process multiple voice and data communication signal samples for communication over IP, ATM, Frame Relay or other packetized network. The four signal processing units can execute processing algorithms in parallel. Each ASSP is flexible and can be programmed to perform many network functions or data/voice processing functions, including voice and data compression/decompression in telecommunications systems (such as CODECs) particularly packetized telecommunication networks, simply by altering the software program controlling the commands executed by the ASSP.

3. Any inquiry concerning this communication or earlier communication from the examiner should be direct to Albert W. Paladini whose telephone number is (571) 272-3748. The examiner can normally be reached from 7:00 to 3:00 PM on Monday, Tuesday, Thursday, and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Leo P. Picard, can be reached on (571) 272-3749. The official fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Albert W. Paladini
Primary Examiner
Art Unit 2125

October 28, 2005